INF4420 Project

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Successive approximation register (SAR) analog to digital converter (ADC)

Project introduction

Data converters are one of the fundamental building blocks in integrated circuit design. Their purpose is to interface the analog and digital domains. Data converters can be realized in many different ways and may be found in a wide variety of applications. One often used ADC topology is the SAR ADC, see Figure 1. This topology uses a DAC, sample and hold, comparator and digital circuitry in order to convert an analog signal into a digital form of representation.
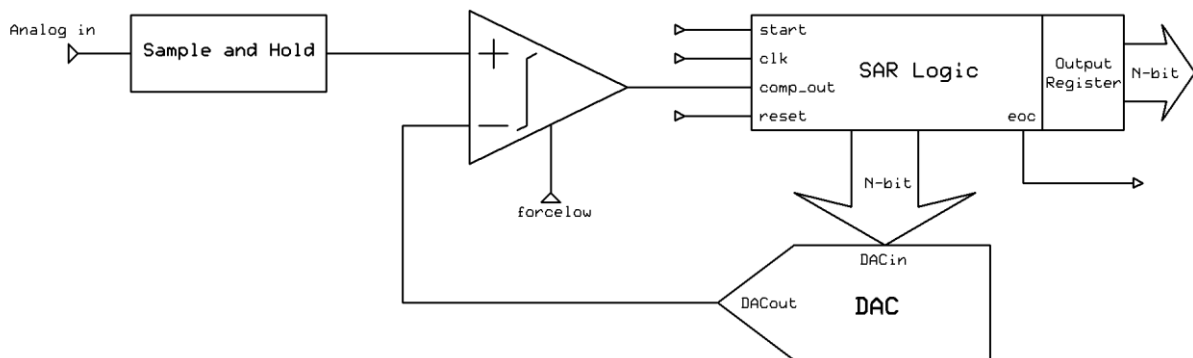

Figure 1) SAR ADC

Your task is to design a *current steering digital to analog converter* and an *output register*, which is going to be implemented in a SAR ADC topology.

There are several (ideal) components supplied that may be used in the project. These components can be found here: */ifi/midgard/h01/amirh/tsmc90nmlp2/INF4420Project*

To get access to these components bring up the Library Manager in Cadence, go to (Edit->Library Path), then type in the library name "INF4420Project" and the library path displayed above. If you want to *edit* the files, copy them to your cadence folder using Library Manager.

The workload in the project is intended for groups consisting of two students.

Task 1: Design a testbench for the DAC and SAR ADC introduction

- Make a suitable testbench for the DAC.
- Write a small report (2 pages maximum) regarding the SAR ADC architecture and include the following in your report:
  - Describe the functionality of a typical SAR ADC architecture.
  - Pros and cons of the SAR ADC architecture.
  - Other aspects that may be relevant.
    (This report may be included in your final report as parts of the introduction or similar)
- Get yourself familiar with the supplied SAR ADC components and implement the *output register* using the supplied (ideal) building blocks.

Task 2: DAC design

Current steering DACs are based on an array of current sources that are switched to the output node depending on the input digital code. There are several different ways of implementing such a topology, however tradeoffs between these topologies should be taken into consideration. This will be up to you as designers to evaluate. The basic concept is illustrated in Figure 2.
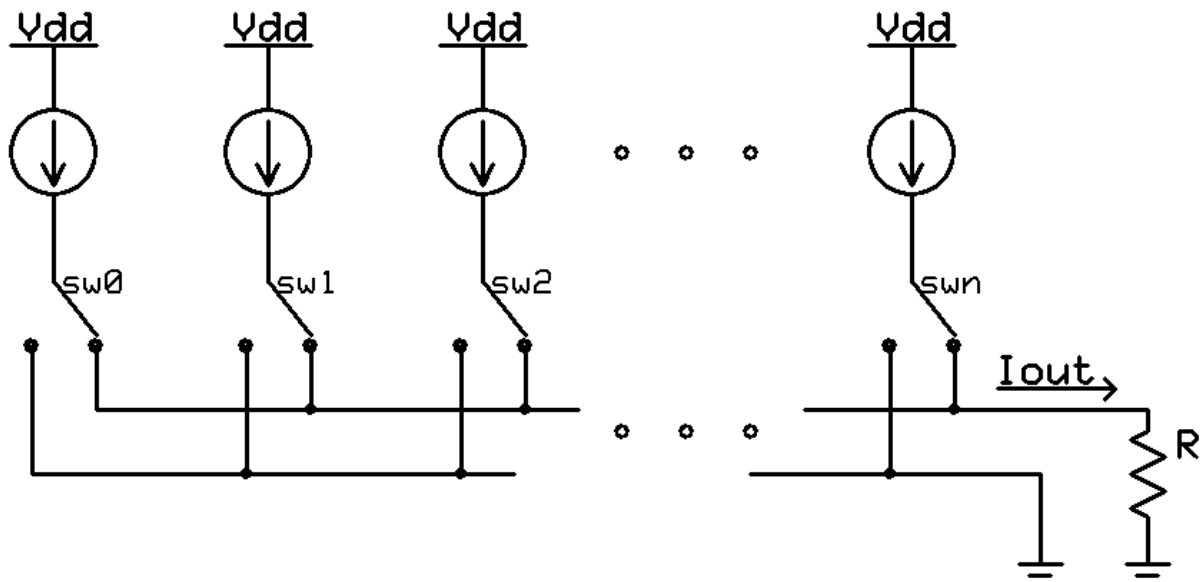

Figure 2) Basic concept

The *minimum* specification requirements for the DAC are:

➢ Minimum 6bit resolution
➢ Sample rate > 8Ms/s
➢ DNL < +/- 0.5LSB
➢ INL < +/- 0.5LSB
➢ Minimum output signal range of 600mV. (i.e 0-600mV)

For this particular implementation the supply voltage is 1.2V and you may assume you have a 1uA current source available for biasing.

There are several other DAC specifications that are important, such as power consumption, settling time etc. Identify these specifications and include them in your final report.

Task 3: Implementation of DAC into SAR ADC

Implement your DAC design into the SAR ADC topology. Make necessary modifications to the ideal components if your implementation has higher specifications then the minimum (for example resolution).

- Assign a ramp up signal to the ADC input and verify that you get corresponding digital values on the ADC output.

Project requirements

Group members must jointly go through the project description and assign work assignments. It must be made visible in the report how the distribution of work has been assigned throughout the project. The following (*but not limited to*) tasks must be addressed before the project can be regarded as complete:

1) It is expected that all circuits/sub-circuits have a schematic and appropriate symbol. The final DAC should be made up of a single symbol.

2) After the DAC schematic is complete and all simulation results (including Monte Carlo simulations) are satisfactory, a layout of the complete system must be made. There are certain issues that are often encountered when doing analog/mixed-signal layout. Find out what they could be and describe them in your final report. Make an effort to implement countermeasures.

3) When you have completed the layout, run Design Rule Check (DRC) and Layout Versus Schematic (LVS). These checks have to be free of errors. The LVS output log must be included in the final report as an appendix.

4) The next step is to do back annotation of parasitic components (R and C) to the schematic view, or parasitic extraction as it is also called. This will result in a netlist with parasitic resistances and capacitances.

5) On the basis of the extracted netlist, you may now do post layout simulations (Monte Carlo simulations included). Her you must carry out the appropriate simulations and compare them with the previous simulation results that were solely based on the schematics.

Report requirements

The final report may be written it the text editor of your choice, but the report must be well organized and easy to read. All central aspects of the project must be supplied by relevant figures and plots. It is important to document/justify the choices you make regarding both the schematic and layout. (Important topics may be; matching, transistor dimensions, choice of components etc.) Plots of all the schematics and the layout, with clearly visible parameters such as dimensions must be included as an appendix for all circuits/sub circuits. References that you may have used in the project must also be included. All schematics and layouts must be made available for inspection, with the exact directory path specified in your final report. Everything must be understandable just from reading the final report.

Submissions and approvals

- Task 1. *Mandatory* hand-in*.*
    - o Schematics (approved by lab advisor) *Deadline February 15.*
- Task 2.
    - o Schematic (approval by lab advisor) *Deadline March 15.*
    - o Layout (approval by lab advisor) *Deadline April 12.*
- Task 3. *Deadline April 19.*
- Final Report. *Deadline May 4.*